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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/518,556	12/22/2004	Richard Michael Taylor	356884.00005-US	8394

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Saul Ewing LLP (Philadelphia)
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EXAMINER
YIGDALL, MICHAEL J

ART UNIT	PAPER NUMBER
2192	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Office Action Summary	10/518,556	TAYLOR, RICHARD MICHAEL
	Examiner	Art Unit	
	Michael J. Yigdall	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2008*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 15-27* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 15-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

1.   This Office action is responsive to Applicant's reply filed on November 7, 2008. Claims

1-12 and 15-27 are pending.

Response to Amendment

2.   The rejection of claims 1-26 under 35 U.S.C. § 101 is withdrawn in view of Applicant's

amendments to the claims.

Response to Arguments

3.   Applicant's arguments have been considered but are moot in view of the new ground(s)

of rejection set forth below. Applicant's amendments to the claims necessitated the new

ground(s) of rejection.

Claim Rejections under 35 U.S.C. § 112

4.   The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the
> subject matter which the applicant regards as his invention.

5.   Claims 1-12 and 15-27 are rejected under 35 U.S.C. § 112, second paragraph, as being

indefinite for failing to particularly point out and distinctly claim the subject matter that

Applicant regards as the invention.

        With respect to claim 1 (currently amended), the claim is ostensibly directed to a method

of generating executable code. However, the claim does not recite any steps involved in the

method that would actually result in the generation of executable code. Accordingly, the claim

does not clearly set forth the metes and bounds of the subject matter that Applicant intends to

encompass. Furthermore, there is insufficient antecedent basis in the claim for "the register

access dependency rules" recited in step (e). The examiner's interpretation is that Applicant

intends such language to refer to the "dependencies between reads and writes to registers"

introduced in step (d).

With respect to claims 2-12, 15-26 (original) and 27 (previously presented), the claims

are dependent upon claim 1 and therefore are indefinite for the same reason(s) as noted above.

Claim Rejections under 35 U.S.C. § 102

6.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form

the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7.   Claim 27 is rejected under 35 U.S.C. § 102(b) as being anticipated by Jan Hoogerbrugge,

"Code Generation for Transport Triggered Architectures" (already of record, "Hoogerbrugge").

With respect to claim 27 (previously presented), Hoogerbrugge teaches a microprocessor

configured to execute code that has been generated using the method of claim 1 (see, for

example, page 2, section 1.1, "Application Specific Processors," which shows such a

microprocessor, and see, for example, pages 4-5, Figure 1.2 and section 1.2, "Transport

Triggered Architectures," which shows the structural limitations that claim 1 implicitly imparts

to the microprocessor of claim 27).

Claim Rejections under 35 U.S.C. § 103

8.   The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9.   Claims 1-12 and 15-27 are rejected under 35 U.S.C. § 103(a) as being unpatentable over

Hoogerbrugge.

       With respect to claim 1 (currently amended), Hoogerbrugge teaches a method of

generating executable code for a configurable microprocessor architecture which has an

instruction set and a plurality of physical data path connections between execution units (see, for

example, pages 43-44, section 3.1, "Overview of the Compiler," which shows generating

executable code for a configurable transport-triggered microprocessor architecture, and see, for

example, pages 4-5, Figure 1.2 and section 1.2, "Transport Triggered Architectures," which

shows that the architecture includes an instruction set and physical data path connections among

functional units), comprising:

       (a) situating individual registers in the data paths between execution units (see, for

example, pages 26-27, "Figure 2.9 shows the general structure of a TTA ...," which shows that

the architecture includes individual registers in data paths among functional units);

(b) updating said registers by explicit management from the instruction set of the processor (see, for example, pages 4-5, section 1.2, "Transport Triggered Architectures," which shows that the update of the registers is managed from the instruction set); and

(c) reading and writing of said registers, whereby said reading and writing is represented in a data flow graph representation of a program being targeted to the processor (see, for example, page 29, Figure 2.12, which shows a data flow graph that represents the reading and writing of the registers);

(d) representing dependencies between reads and writes to registers as edges in the graph (see, for example, pages 19-21, "Data dependences");

(e) detecting, by the presence of cycles within the graph, graphs that invalidate the register access dependency rules (see, for example, pages 89-90, section 5.1.1, "Cyclic Data Dependency Graphs").

Hoogerbrugge further teaches performing register allocation on the graph (see, for example, pages 56-57, "Register allocation is performed …"), but does not explicitly describe:

(f) performing cyclic detection after each individual register allocation performed on the graph to detect an allocation which is illegal.

Nonetheless, those of ordinary skill in the art would have been prompted to implement the teachings of Hoogerbrugge such that each register allocation is legal. Indeed, Hoogerbrugge further suggests:

(g) using the cycle detection mechanism to force alternative allocation decisions to be made to avoid cyclic graphs and direct the allocation to an acyclic and thus legal allocation (see, for example, pages 56-57, "A false dependence prevention graph (FDPG) is built …").

Thus, the claimed subject matter would have been obvious to those of ordinary skill in the art at the time the invention was made.

With respect to claim 2 (original), the rejection of claim 1 is incorporated, and Hoogerbrugge further teaches that the number of registers associated with particular execution units is configurable (see, for example, page 48, Figure 3.3).

With respect to claim 3 (original), the rejection of claim 1 is incorporated, and Hoogerbrugge further teaches that the target architecture is specified in an input file (see, for example, pages 46-47, "The machine description file …").

With respect to claim 4 (original), the rejection of claim 1 is incorporated, and Hoogerbrugge further teaches that certain units may only be connected to a subset of other execution units in the architecture (see, for example, page 4, Figure 1.2).

With respect to claim 5 (original), the rejection of claim 4 is incorporated, and Hoogerbrugge further teaches that there is a central register file but only a subset of the execution units in the system can directly communicate with it (see, for example, pages 32-34, section 2.3.6, "The Interconnection Network").

With respect to claim 6 (original), the rejection of claim 3 is incorporated, and Hoogerbrugge further teaches that the input program is initially represented as a sequence of operations that can be performed by execution units present in the target architecture (see, for example, page 46, "The back-end starts with reading the sequential program …").

With respect to claim 7 (original), the rejection of claim 6 is incorporated, and Hoogerbrugge further teaches that the inputs to and results from these basic instructions may be communicated via a central register file (see, for example, pages 26-27, "Figure 2.9 shows the general structure of a TTA …").

With respect to claim 8 (original), the rejection of claim 7 is incorporated, and Hoogerbrugge further teaches that the code sequence may be optimised to reduce the communication required with the central register file (see, for example, page 115, section 6.2.4, "TTA Specific Optimizations").

With respect to claim 9 (original), the rejection of claim 8 is incorporated, and Hoogerbrugge further teaches that multiple reads of a given register file value may be transformed into a single read with suitable communication of the same data to other consumers of the data value (see, for example, pages 39-40, "Operand sharing").

With respect to claim 10 (original), the rejection of claim 8 is incorporated, and Hoogerbrugge further teaches that pairs of central register file writes and reads may be transformed to use direct communication between the generating and consuming operations (see, for example, page 40, "Socket sharing").

With respect to claim 11 (original), the rejection of claim 1 is incorporated, and Hoogerbrugge further teaches that the data flow graph is transformed so that data edges correspond to physical connections in the architecture (see, for example, pages 139-141, section 7.1.2, "Connectivity Optimization").

With respect to claim 12 (original), the rejection of claim 11 is incorporated, and
Hoogerbrugge further teaches that additional nodes may be inserted into the graph to represent
the copying of data values where there is no physical connection corresponding to the graph data
flow (see, for example, pages 100-102, section 5.2.3, "Delay Lines").

With respect to claim 15 (original), the rejection of claim 1 is incorporated, and
Hoogerbrugge further teaches that an idealised form of the graph is generated that assumes the
availability of unrestricted connectivity in the architecture (see, for example, pages 139-141,
section 7.1.2, "Connectivity Optimization").

With respect to claim 16 (original), the rejection of claim 15 is incorporated, and
Hoogerbrugge further teaches that the idealised form of the graph is used to influence the
binding of operations to physical execution units in the architecture (see, for example, pages 139-
141, section 7.1.2, "Connectivity Optimization").

With respect to claim 17 (original), the rejection of claim 1 is incorporated, and
Hoogerbrugge further teaches that special edges within the graph represent communication of
data via a central register file (see, for example, pages 19-21, "Data dependences").

With respect to claim 18 (original), the rejection of claim 17 is incorporated, and
Hoogerbrugge further teaches that operations from different basic blocks may be represented in a
single graph (see, for example, pages 69-70, section 4.1, "Scheduling Scopes").

With respect to claim 19 (original), the rejection of claim 1 is incorporated, and Hoogerbrugge further teaches that individual operations in the graph are bound to particular execution unit instances (see, for example, pages 61-63, section 3.2.3, "Resource Assignment").

With respect to claim 20 (original), the rejection of claim 19 is incorporated, and Hoogerbrugge further teaches that the unit binding uses an estimate of the delay caused by transporting operands to and results from the operation as a factor in the allocation (see, for example, pages 28-30, section 2.3.2, "An Example").

With respect to claim 21 (original), the rejection of claim 20 is incorporated, and Hoogerbrugge further teaches that the transport cost is dependent on the structure of connectivity between the operations in the graph (see, for example, pages 139-141, section 7.1.2, "Connectivity Optimization").

With respect to claim 22 (original), the rejection of claim 1 is incorporated, and Hoogerbrugge further teaches that the graph may be updated as new physical paths are added to the architecture in order to reduce the graph height to allow shorter code schedules (see, for example, pages 63-64, section 3.2.4, "Scheduling an Operation").

With respect to claim 23 (original), the rejection of claim 1 is incorporated, and Hoogerbrugge further teaches that individual execution units are controlled by particular bits within the overall execution word (see, for example, page 27, Figure 2.10).

With respect to claim 24 (original), the rejection of claim 23 is incorporated, and Hoogerbrugge further teaches that certain bits in the execution word may be used to control more

than a single execution unit (see, for example, page 91, "… operations can be performed by multiple FU types …").

With respect to claim 25 (original), the rejection of claim 24 is incorporated, and Hoogerbrugge further teaches that the allocation of bits in the execution word to particular execution units is optimised as the architecture is generated (see, for example, pages 136-139, section 7.1.1, "Resource Optimization").

With respect to claim 26 (original), the rejection of claim 25 is incorporated, and Hoogerbrugge further teaches that the usage of individual execution units is used to influence the allocation of the execution word (see, for example, pages 134-135, section 7.1, "The Design Process").

With respect to claim 27 (previously presented), the rejection of claim 1 is incorporated, and Hoogerbrugge further teaches a microprocessor configured to execute code that has been generated using the method of claim 1 (see, for example, page 2, section 1.1, "Application Specific Processors," which shows such a microprocessor).

Conclusion

10.   Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this

final action.

11.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Michael J. Yigdall whose telephone number is 571-272-3707.

The examiner can normally be reached on Monday to Friday from 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Tuan Q. Dam can be reached on 571-272-3695. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

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would like assistance from a USPTO Customer Service Representative or access to the

automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Michael J. Yigdall
Primary Examiner
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